

Form PTO-1449

U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICEATTY. Docket NO.  
M122-1343

SERIAL NO.

LIST OF ART CITED BY APPLICANT  
(Use several sheets if necessary)APPLICANT  
Robert Kerr et al.

FILING DATE

GROUP

## U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Applicable
PC	AA	5,162,890	11/92	Butler	257	306	
PC	AB	5,166,096	11/92	Cote et al.	437	195	
PC	AC	5,173,752	12/92	Motonami et al.	257	309	
PC	AD	5,272,367	12/93	Dennison et al.	257	306	
PC	AE	5,317,193	05/94	Watanabe	257	774	
PC	AF	5,444,003	08/95	Wang et al.	437	31	
PC	AG	5,510,648	04/96	Davies et al.	257	657	
PC	AH	5,547,892	08/96	Wuu et al.	437	52	
PC	AI	5,552,620	09/96	Lu et al.	257	302	
PC	AJ	5,576,243	11/96	Wuu et al.	437	195	
PC	AK	5,612,240	03/97	Chang	437	44	

## FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Subclass	Translation	
							Yes	No
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## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

PC	AR		Stanley Wolf, Silicon Processing for the VLSI Era, Volume 3: The Submicron MOSFET, Lattice Press, pg. 136-138, 232-234, 1995
	AS		
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EXAMINER

PHAT X. CAO

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U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
PC	AA	5,652,174	07/97	Wuu et al.	437	60		
PU	AB	5,668,021	09/97	Subramanian et al.	438	282		
PU	AC	5,710,450	01/98	Chau et al.	257	344		
PU	AD	5,736,441	04/98	Chen	438	255		
PU	AE	5,808,320	09/98	Dennison	257	68		
PU	AF	5,811,350	09/98	Dennison	438	597		
PU	AG	5,885,890	03/99	Dennison	438	597		
PU	AH	5,243,219	09/93	Katayama	287	740		
PU	AI	5,731,610	03/98	Rhodes	257	309		
PU	AJ	5,206,187	04/93	Doan et al.	437	192		
PU	AK	5,763,321	06/98	Ohshima et al.	438	618		
FOREIGN PATENT DOCUMENTS								
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					FILING DATE		GROUP	
U.S. PATENT DOCUMENTS								
*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate	
PL	AA	5,707,883	01/98	Tabara	437	40		
PU	AB	5,686,331	11/97	Song	437	41		
PU	AC	5,960,318	09/99	Peschke et al.	438	637		
PU	AD	5,747,359	05/98	Yuan et al.	437	186		
PU	AE	5,946,578	08/99	Fujii	438	300		
PU	AF	5,912,492	06/99	Chang et al.	257	344		
PU	AG	5,897,350	04/99	Lee et al.	438	238		
PU	AH	5,891,780	04/99	Hasegawa et al.	438	278		
PU	AI	5,864,155	01/99	Melzner	257	306		
PU	AJ	4,281,448	08/81	Barry et al.	29	577		
PU	AK	5,930,618	07/99	Sun et al.	438	240		
FOREIGN PATENT DOCUMENTS								
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Robert Kerr et al.

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*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
PC	AA	5,591,662	01/97	Zambrano	437	57	
PU	AB	5,899,712	05/99	Choi et al.	438	163	
PU	AC	4,936,928	06/90	Shaw et al.	148	33.4	
PU	AD	5,970,360	10/99	Cheng et al.	438	398	
PU	AE	5,858,832	01/99	Pan	438	230	
PU	AF	5,866,927	02/99	Cho et al.			
PU	AG	5,827,770	10/98	Rhodes	438	396	
	AH						
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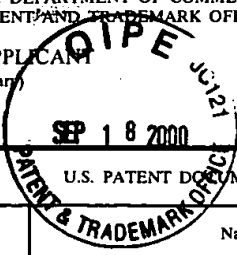
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U.S. DEPARTMENT OF COMMERCE  
PATENT AND TRADEMARK OFFICE

ATTY. DOCKET  
M122-1343

SERIAL NO.  
09/512,978

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APPLICANT  
Robert Kerr et al.

FILING DATE  
2/24/2000

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*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
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OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

pc	AR	Wolf, S., "Silicon Processing for the VLSI Era," Vol. 3: The Submicron MOSFET, Lattice Press 1995, pp. 634-636.
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U.S. PATENT DOCUMENTS

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
pc	AA	5,895,269	4/99	Wang et al.	438	675	
pc	AB	6,093,609	7/00	Chuang	438	286	
	AC						
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	AO							
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## OTHER REFERENCES (including Author, Title, Date, Pertinent Pages, Etc.)

pc	AR		Gray, Paul R. et al., "Analysis and Design of Analog Integrated Circuits," Third Edition, 1993, John Wiley and Sons, page 169 -- specifically the 2 <sup>nd</sup> paragraph
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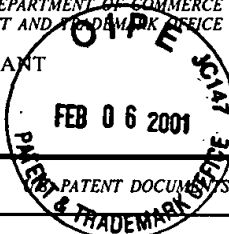
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MI22-1343SERIAL NO.  
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Micron Technology, Inc.FILING DATE  
February 24, 2000GROUP  
2825

*Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
PC	AA	5,874,359	2/23/99	Liaw et al.	438	640	
	AB						
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*Examiner Initial	Document Number	Date	Name	Class	Subclass	Filing Date If Appropriate
pc	AA 6,133,103	10/2000	Lee et al.	438	276	
pc	AB 6,097,103	08/2000	Ishigaki	257	903	
	AC					
	AD					
	AE					
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pc	AR	Shenai, K., "A high-density, self-aligned power MOSFET structure fabricated using sacrificial spacer technology" Electron Devices, IEEE Transactions on Electron Devices, Vol. 39, Issue 5, May 1992, pps 1252-1255.
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